METHOD OF SIMULATING ADDITIONAL PROCESSORS IN A SIMD PARALLEL PROCESSOR ARRAY

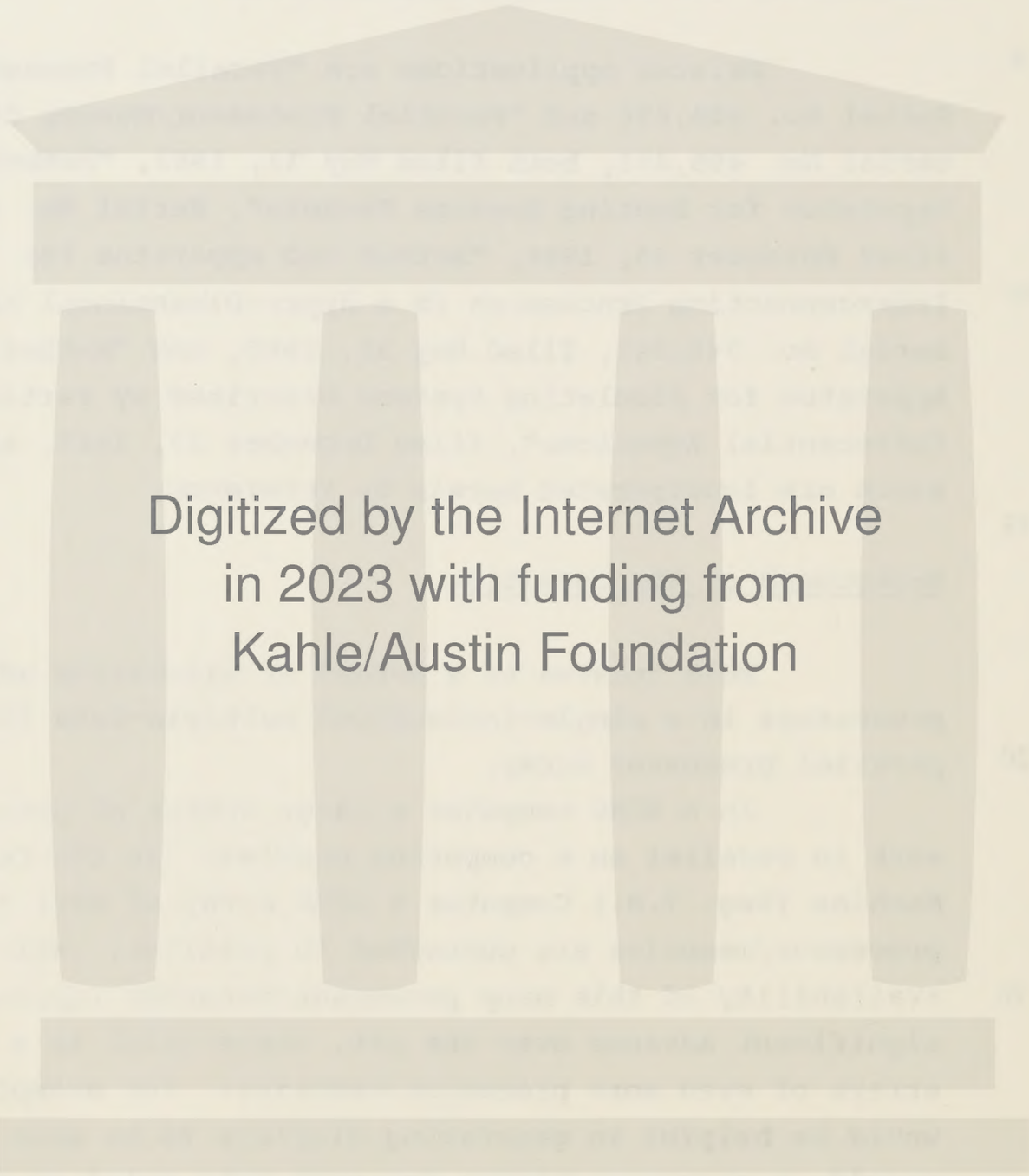
Cross Reference to Related Applications

Related applications are "Parallel Processor", Serial No. 499,474 and "Parallel Processor/Memory Circuit", Serial No. 499,471, both filed May 31, 1983, "Method and Apparatus for Routing Message Packets", Serial No. 671,835, filed November 15, 1984, "Method and Apparatus for Interconnecting Processors in a Hyper-Dimensional Array", Serial No. 740,943, filed May 31, 1985, and "Method and Apparatus for Simulating Systems Described by Partial Differential Equations", filed December 27, 1985, all of which are incorporated herein by reference.

Background of the Invention

This relates to a method of simulating additional processors in a single-instruction multiple-data (SIMD) parallel processor array.

In a SIMD computer a large number of processors work in parallel on a computing problem. In the Connection Machine (Reg. T.M.) Computer a SIMD array of over 32,000 processor/memories are connected in parallel. While the availability of this many processor/memories represents a significant advance over the art, there still is a need for arrays of even more processor/memories. For example, it would be helpful in generating displays to be able to provide a processor/memory for each data point on pixel in the display. To provide a high resolution display of 1000 x 1000 pixels with such capability, it is necessary to provide 1,000,000 processor/memories. Similar numbers are likely to be needed for devices which simulate vision and other devices of interest to artificial intelligence



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studies. Other applications such as the simulations of fluid media described in "Method and Apparatus for Simulating Systems Described by Partial Differential Equations" also need enormous numbers of processor/memories if use of these inventions is to be practical.

Summary of the Invention

We have discovered that additional processors can be simulated in a SIMD computer by dividing the memory associated with each processor into a plurality of sub-memories and then operating on each sub-memory in succession as if it were associated with a separate processor. Thus, a first instruction or set of instructions is applied to all the processors of the array to cause at least some processors to process data stored at a first location or locations in the first sub-memory. Thereafter, the same first instruction or set of instructions is applied to all the processors of the array to cause at least some processors to process data stored at the same first location in a second sub-memory. And so forth for each of the sub-memories.

By operating a SIMD computer in this fashion, it is possible in effect to vary the number of processors in the array so as to provide the number of processors required for a problem. This permits programs that require large numbers of processors to run on computers that do not have that many physical processors. It makes it possible to perform computational problems such as those associated with the generation of a display with greater resolution than would otherwise be possible. In the case of the simulation of systems described by partial differential equations, the technique of the present invention makes it possible to compute data for over 4,000,000 points in an array using only 32,768 processors.

Brief Description of the Drawings

These and other objects, features and advantages of our invention will be more readily apparent from the following detailed description of a preferred embodiment of the invention in which:

Figs. 1 and 2 depict in schematic form details of a SIMD processor preferably used in the practice of the invention; and

Fig. 3 is a flow chart illustrating the practice of the invention.

Detailed Description of the Preferred Embodiment

The present invention is intended to be implemented in a single instruction multiple data (SIMD) computer such as the Connection Machine Computer described in detail in application Serial No. 499,474.

As shown in Fig. 1A of that application which is reproduced in Fig. 1, the computer system comprises a mainframe computer 10, a microcontroller 20, an array 30 of parallel processing integrated circuits 35, a data source 40, a first buffer and multiplexer/demultiplexer 50, first, second, third and fourth bidirectional bus control circuits 60, 65, 70, 75, a second buffer and multiplexer/demultiplexer 80, and a data sink 90. Mainframe computer 10 may be a suitably programmed commercially available general purpose computer such as a VAX (TM) computer manufactured by Digital Equipment Corp. Microcontroller 20 is an instruction sequencer of conventional design for generating a sequence of instructions that are applied to array 30 by means of a thirty-two bit parallel bus 22. Microcontroller 20 receives from array 30 a signal on line 26. This signal is a general purpose or GLOBAL signal that can be used for data output

and status information. Bus 22 and line 26 are connected in parallel to each IC 35. As a result, signals from microcontroller 20 are applied simultaneously to each IC 35 in array 30 and the signal applied to microcontroller 20 on line 26 is formed by combining the signal outputs from all of ICs 35 of the array.

In the embodiment of the Connection Machine Computer used in the practice of the present invention, array 30 contains 2048 ($=2^{11}$) identical ICs 35; and each IC 35 contains 16 ($=2^4$) identical processor/memories 36. Thus, the entire array 30 contains 32,768 ($=2^{15}$) identical processor/memories 36.

Processor/memories 36 are organized and interconnected in two geometries. One is a conventional two-dimensional grid pattern in which the processor/memories are organized in a rectangular array of 128 x 256 processor/memories and connected to their four nearest neighbors in the array. The other is a Boolean-cube of fifteen dimensions.

To connect each processor/memory to its four nearest neighbors, the individual processor/memories are connected by electrical conductors between adjacent processor/memories in each row and each column of the grid as shown in Figs. 6A and 7A of the '474 application; and the four nearest neighbors of an IC except those on the edges of the array will be recognized to be the four ICs immediately adjacent that IC on the North, East, South and West.

Connections to the fifteen nearest neighbors of each processor/memory in the Boolean-cube are made by means of electrical conductors and routers. Details of the wiring scheme are set forth in the '943 application referenced above. Details of the router are set forth in the '474 application.

An illustrative processor/memory 36 is disclosed in greater detail in Fig. 2 which is the same as Fig. 7A of the '474 application. As shown in Fig. 2, the processor/memory comprises random access memory (RAM) 250, arithmetic logic unit (ALU) 280 and flag controller 290. The ALU operates on data from three sources, two registers in the RAM and one flag input, and produces two outputs, a sum output that is written into one of the RAM registers and a carry output that is made available to certain registers in the flag controller as well as to certain other processor/memories.

The inputs to RAM 250 are busses 152, 154, 156, 158, a sum output line 285 from ALU 270, the message packet input line 122 from communication interface unit (CIU) 180 of Fig. 6B of the '474 application and a WRITE ENABLE line 298 from flag controller 290. The outputs from RAM 250 are lines 256, 257. The signals on lines 256, 257 are obtained from the same column of two different registers in RAM 250, one of which is designed Register A and the other Register B. Busses 152, 154, 156, 158 address these registers and the columns therein in accordance with the instruction words from microcontroller 20. Illustratively, RAM 250 has a memory capacity of 4096 bits.

Flag controller 290 is an array of eight one-bit D-type flip-flops 292, a two-out-of-sixteen selector 294 and some logic gates. The inputs to flip-flops 292 are a carry output signal from ALU 280, a WRITE ENABLE signal on line 298 from selector 294, and the eight lines of bus 172 from programmable logic array (PLA) 150 of Fig. 6B of the '474 application. Lines 172 are address lines each of which is connected to a different one of flip-flops 292 to select the one flip-flop into which a flag bit is to be written. The outputs of flip-flops 292 are applied to selector 294.

The inputs to selector 294 are up to sixteen flag signal lines 295, eight of which are from flip-flops 292, and the sixteen lines each of busses 174, 176. Again, lines 174 and 176 are address lines which select one of the flag signal lines for output or further processing. Selector 294 provides outputs on lines 296 and 297 that are whichever flags have been selected by address lines 174 and 176, respectively. The flags are defined in detail in Table IV of the '474 application.

ALU 280 comprises a one-out-of-eight decoder 282, a sum output selector 284 and a carry output selector 286. As detailed in the '474 application, this enables it to produce sum and carry outputs for many functions including ADD, logical OR and logical AND. ALU 280 operates on three bits at a time, two on lines 256, 257 from Registers A and B in RAM 250 and one on line 296 from flag controller 290. The ALU has two outputs: a sum on line 285 that is written into Register A of RAM 250 and a carry on line 287 that may be written into a flag register 292 and applied to the North, East, South, West and DAISY inputs of the other processor/memories 36 to which this processor/memory is connected.

In accordance with the present invention, each processor/memory can be divided into several units that function identically. In effect, each unit operates as a separate processor/memory sharing the RAM, ALU and flag controller of one physical processor/memory. The number of such units that can be implemented in one physical processor/memory depends on the memory requirements for each unit.

The subdivision of one physical processor/memory into several is accomplished by partitioning the memory in each physical processor/memory in the same fashion and providing in microcontroller 20 of Fig. 1 the capacity of having each physical processor memory operate first on one

portion of the partitioned memory, then on the next portion of the partitioned memory and so on through each subdivision of the memory. A flow chart illustrating this process is set forth in Fig. 3.

Subdivision of the memory is readily accomplished. For example, in the present design of the Connection Machine Computer, each RAM 250 contains 4096 bits or 512 bytes of eight bits each. Illustratively, each byte has a separate memory location or address from 000 through 511. To subdivide the memory into four sub-memories, memory locations 000 through 127 are assigned to first sub-memory, memory locations 128 through 255 to a second sub-memory, memory locations 256 through 383 to a third sub-memory, and memory locations 384 through 511 to a fourth sub-memory. The memory can be divided into smaller sub-divisions if desired.

The same memory location in each sub-memory relative to the first memory location is used exactly the same way in each sub-memory. Thus, if data specifying the degrees, minutes and seconds of an angle are stored in first, second and third memory locations 000, 001, and 002 of the first sub-memory, data specifying the degrees, minutes and seconds of an angle are also stored in first, second and third memory locations 128, 129, 130 of the second sub-memory, in first, second and third memory locations 256, 257, 258 of the third sub-memory, and in first second and third memory locations 384, 385, 386 of the fourth sub-memory.

The sequence of operations performed on each portion of the partitioned memory is the same whether it involve a single operation or several. The capability of advancing from one portion of the partitioned memory to the next portion may be achieved in different ways. For example, all addressing in the programs specified by the controller can be relative with respect to the first memory

address of each subdivided unit of memory. Alternatively, the memory addresses used in the program may be specified in relative terms in the program and then these addresses may be incremented when advancing from one portion of the partitioned memory to the next.

As will be apparent to those skilled in the art, numerous modifications may be made within the scope of the above described invention.

What is claimed is:

1. In a single-instruction multiple-data (SIMD) parallel processor comprising a controller and an array of processors controlled in parallel by said controller, each processor comprising an identical input, an identical output, an identical processing element and an identical memory associated with each processing element, the processing element operating in accordance with instructions provided by said controller on data provided by its input and associated memory to produce data at its output, a method of simulating the presence of additional processors in the array comprising the steps of:

a) subdividing the memory elements associated with the processing elements in identical fashion to form a plurality of sub-memories associated with each processing memory,

b) providing at least a first instruction or first set of instructions from the controller to the processors to cause the processing elements of at least some processors each to process data stored at a first location in a first sub-memory associated with the processing element, and

c) at a subsequent time, providing said first instruction or first set of instructions from the controller to the processors to cause the processing elements of at least some processors each to process data stored at the same first location in a second sub-memory associated with the processor.

2. The method of claim 1 further comprising the steps of repeating steps (b) and (c) on new data stored at the same first locations in the first and second sub-memories.

3. The method of claim 1 further comprising the steps of repeating steps (b) and (c) on data stored at a second location in the first and second sub-memories.

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DECLARATION AND POWER OF ATTORNEY

PENNIE & EDMONDS DOCKET NO.
1947-013

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor if only one name is listed at 201 below, or an original, first and joint inventor if plural names are listed at 201 et seq. below, of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF SIMULATING ADDITIONAL PROCESSORS IN A SIMD PARALLEL PROCESSOR ARRAY

the specification of which:

☒ is attached hereto ☐ was filed on ..... as Application Serial No. .....
(for declaration not accompanying application)

with amendment(s) filed None
(If applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/§172 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C 119/172
None			YES____ NO____
			YES____ NO____
			YES____ NO____
			YES____ NO____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS		
		PATENTED	PENDING	ABANDONED
None				

POWER OF ATTORNEY: As a named inventor, I hereby appoint Frank F. Scheck (Reg. No. 17761), S. Leslie Misrock (Reg. No. 18872), Clyde C. Metzger (Reg. No. 18081), Harry C. Jones, III (Reg. No. 20280), Berj A. Terzian (Reg. No. 20060), Gerald J. Flintoft (Reg. No. 20823), David Weild, III (Reg. No. 21094), Jonathan A. Marshall (Reg. No. 24614), John E. Kidd (Reg. No. 19916), Joseph V. Colaianni (Reg. No. 20019), Keith E. Mullenger (Reg. No. 20054), Charles E. McKenney (Reg. No. 22795), Phillip T. Shannon (Reg. No. 24278), Barry D. Rein (Reg. No. 22411), Stanton T. Lawrence, III (Reg. No. 25736), Francis E. Morris (Reg. No. 24615), Walter G. Marple, Jr. (Reg. No. 28323), Joseph J. Catanzaro (Reg. No. 25837), Charles E. Miller (Reg. No. 24576), Gidon D. Stern (Reg. No. 27469), John J. Lauter, Jr. (Reg. No. 27814), Brian M. Poissant (Reg. No. 28462), Brian D. Coggio (Reg. No. 27624), Rory J. Radding (Reg. No. 28749), and Samuel B. Smith, Jr. (Reg. No. 22278), whose address is Pennie & Edmonds, 1155 Avenue of the Americas, New York, New York 10036, and each of them, my attorneys, to prosecute this application, and to transact all business in the Patent and Trademark Office connected therewith.

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PENNIE & EDMONDS DOCKET NO
1947-013

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	RESIDENCE & CITIZENSHIP	CITY: Somerville	STATE OR FOREIGN COUNTRY: Massachusetts	COUNTRY OF CITIZENSHIP: United States	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: 1006 Broadway	CITY: Somerville	STATE OR COUNTRY: Massachusetts	ZIP CODE: 02144
205	FULL NAME OF INVENTOR	LAST NAME:	FIRST NAME:	MIDDLE NAME:	
	RESIDENCE & CITIZENSHIP	CITY:	STATE OR FOREIGN COUNTRY:	COUNTRY OF CITIZENSHIP:	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS:	CITY:	STATE OR COUNTRY:	ZIP CODE:
206	FULL NAME OF INVENTOR	LAST NAME:	FIRST NAME:	MIDDLE NAME:	
	RESIDENCE & CITIZENSHIP	CITY:	STATE OR FOREIGN COUNTRY:	COUNTRY OF CITIZENSHIP:	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS:	CITY:	STATE OR COUNTRY:	ZIP CODE:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201: W. Hillis	SIGNATURE OF INVENTOR 202: Clifford Lasser	SIGNATURE OF INVENTOR 203: Brewster Kahle
DATE: 2/13/86	DATE: 2/12/1986	DATE: 2/7/86
SIGNATURE OF INVENTOR 204: Karl Sims	SIGNATURE OF INVENTOR 205:	SIGNATURE OF INVENTOR 206:
DATE: 2/6/86	DATE:	DATE:

PE 1B

ABSTRACT

METHOD OF SIMULATING ADDITIONAL PROCESSORS IN A SIMD PARALLEL PROCESSOR ARRAY

A method is described for simulating additional processors in a SIMD computer by dividing the memory associated with each processor into a plurality of sub-memories and then operating on each sub-memory in succession as if it were associated with a separate processor. Thus, a first instruction or set of instructions is applied to all the processors of the array to cause at least some processors to process data stored at a first location or locations in the first sub-memory. Thereafter, the same first instruction or set of instructions is applied to all the processors of the array to cause at least some processors to process data stored at the same first location in a second sub-memory. And so forth for each of the sub-memories. By operating a SIMD computer in this fashion, it is possible in effect to vary the number of processors in the array so as to provide the number of processors required for a problem.

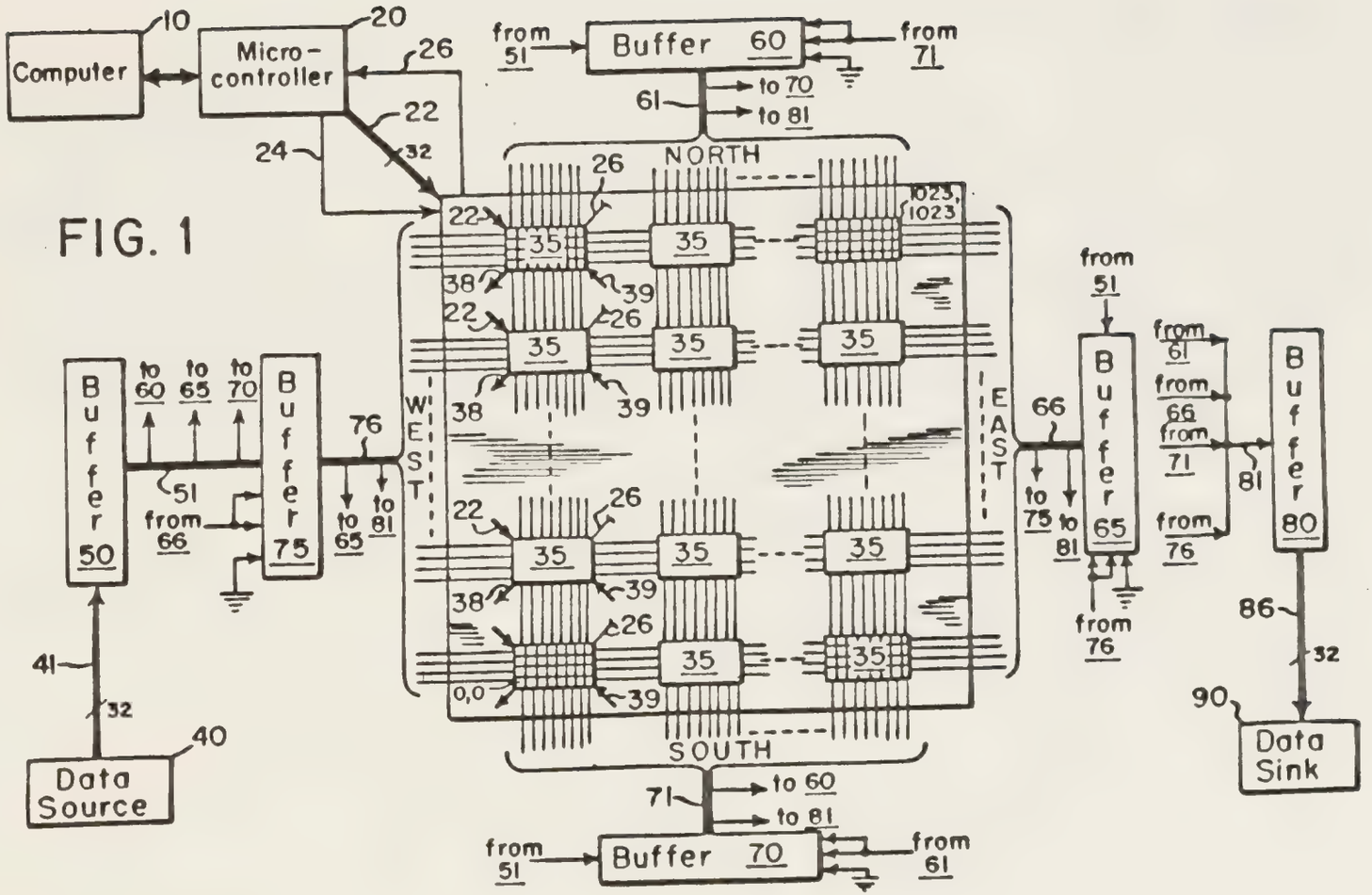


FIG. 1

1947-013 (1-3)

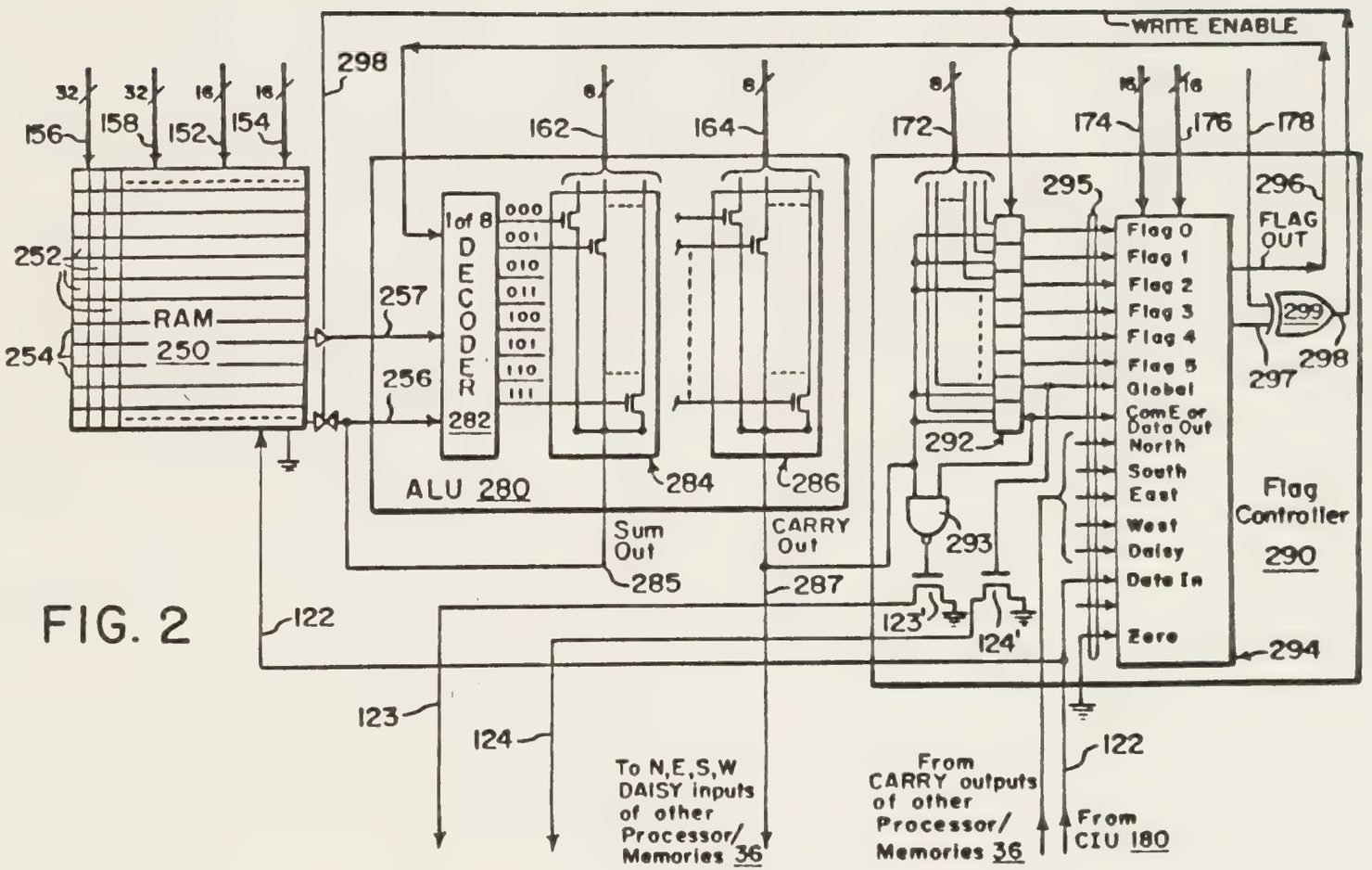
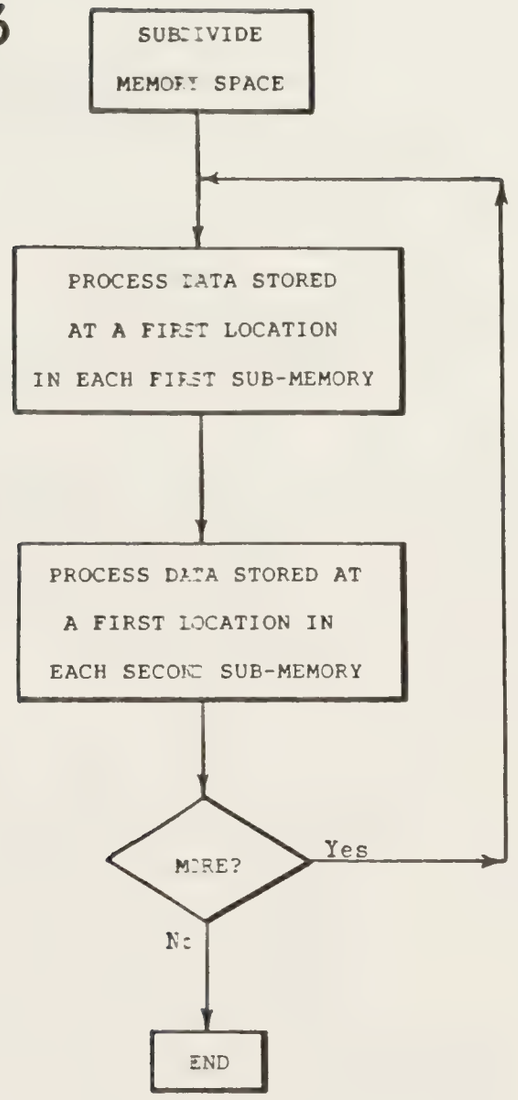

WRITE ENABLE
298
32
32
16
16
156
158
152
154
252
254
RAM
250
257
256
1 of 8
DECODER
282
000
001
010
011
100
101
110
111
8
8
162
164
ALU 280
284
286
Sum Out
285
CARRY Out
287
8
8
172
174
176
178
295
296
FLAG OUT
Flag 0
Flag 1
Flag 2
Flag 3
Flag 4
Flag 5
Global
Comp or Data Out
North
South
East
West
Daisy
Data In
Zero
299
297
298
292
293
Flag Controller
290
294
123'
124'
122
123
124
To N,E,S,W DAISY inputs of other Processor/ Memories 36
From CARRY outputs of other Processor/ Memories 36
122
From CIU 180

FIG. 2

1947-013(3-3)

FIG. 3



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: ☒ Application of: W. Daniel Hillis et al.
☐ Patent of:

☐ Serial No.: Group Art Unit:
☐ Patent No.:

☒ Filed: of even date herewith Examiner:
☐ Issued:

For: METHOD OF SIMULATING ADDITIONAL PROCESSORS IN A SIMD PARALLEL PROCESSOR ARRAY

Attorney Docket No.: 1947-013

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
[37 CFR 1.9(f) and 1.27(c)]—Small Business Concern

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I hereby declare that I am

☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of concern ..... Thinking Machines Corporation .....
Address of concern .... 245 First Street .....
..... Cambridge, Massachusetts 02142 .....

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern and/or there is an obligation under contract or law by the inventor(s) to convey rights to the small business concern with regard to the invention, entitled METHOD OF SIMULATING ADDITIONAL PROCESSORS IN A SIMD PARALLEL PROCESSOR ARRAY
by inventor(s) W. Daniel Hillis et al.
described in

☒ the specification filed herewith
☐ application serial no. ....., filed .....
☐ patent no. ....., issued .....

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

FULL NAME.....

ADDRESS.....

.....

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME.....

ADDRESS.....

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FULL NAME.....

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I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28 (b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

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Name of person signing Henry Hendler

Title of person other than owner President

Address of person signing Thinking Machines
245 First Street, Cambridge, Massachusetts 02142

Signature Henry Hendler Date Feb 14 1986

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

PE-SE 2B

ASSIGNMENT

WHEREAS, WE, W. Daniel Hillis, Clifford Lasser, Brewster Kahle and Karl Sims ASSIGNORS, citizens of the United States residing at 543 Green Street, No. 1, Cambridge, Massachusetts 02139, 85 Gainsborough Street, Boston, Massachusetts 02115, 1006 Broadway, Somerville, Massachusetts 02144, and 1006 Broadway, Somerville, Massachusetts 02144, respectively, are the inventors of the invention in

METHOD OF SIMULATING ADDITIONAL PROCESSORS IN A SIMD PARALLEL PROCESSOR ARRAY

for which we have executed an application for a Patent of the United States, of even date herewith, and

WHEREAS, Thinking Machines Corporation, a corporation of the State of Delaware, having place of business at 245 First Street, Cambridge, Massachusetts 02142, ASSIGNEE is desirous of obtaining the entire right, title and interest in whatever right, title and interest we now have in, to and under the said invention and the said application:

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to us in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, we, the ASSIGNORS, have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said ASSIGNEE, its successors, legal representatives and assigns, the entire right, title and interest in, to and under the said invention, and the said United States application and all divisions, renewals and continuations thereof, and all Patents of the United States which may be granted thereon and all reissues and extensions thereof; and all applications for industrial property protection, including, without limitation, all applications for patents, utility models, and designs which may hereafter be filed for said invention in any country or countries foreign to the United States, together with the right to file such applications and the right to claim for the same the priority rights derived from said United States application under the Patent Laws of the United States, the International Convention for the Protection of Industrial Property, or any other international agreement or the domestic laws of the country in which any such application is filed, as may be applicable; and all forms of industrial property protection, including, without limitation, patents, utility models, inventors' certificates and designs which may be granted for said invention in any country or countries foreign to the United States and all extensions, renewal and reissues thereof;

AND WE HEREBY authorize and request the Commissioner of Patents and Trademarks of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents or other evidence or forms of industrial

property protection on applications as aforesaid, to issue the same to the said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE HEREBY covenant and agree that we have full right to convey the entire interest herein assigned, and that we have not executed, and will not execute, any agreement in conflict herewith.

AND WE HEREBY further covenant and agree that we will communicate to said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said invention, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing, reissue and foreign applications, make all rightful oaths, and generally do everything possible to aid the said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper protection for said invention in all countries.

IN TESTIMONY WHEREOF, We hereunto set out hands and seals the day and year set opposite our respective signatures.

Date 2/13/86, 19__ _____ L.S.

Date 2/12/86, 19__ _____ L.S.

Date 2/7/86, 19__ _____ L.S.

Date 2/8/86, 19__ _____ L.S.

On this 13th day of February, 1986, before me, a Notary Public in and of the State and County aforesaid, personally appeared W. DANIEL Hillis, to me known and known to me to be the person of that name, who signed and sealed the foregoing instrument, and he acknowledged the same to be his free act and deed.

Barbara B Wollen,
Notary Public

On this 13th day of February, 1986, before me, a Notary Public in and of the State and County aforesaid, personally appeared Clift LASSER, to me known and known to me to be the person of that name, who signed and sealed the foregoing instrument, and he acknowledged the same to be his free act and deed.

Barbara B. Wollam,
Notary Public

On this 13th day of February, 1986, before me, a Notary Public in and of the State and County aforesaid, personally appeared BREWSTER KAHLE, to me known and known to me to be the person of that name, who signed and sealed the foregoing instrument, and he acknowledged the same to be his free act and deed.

Barbara B. Wollam,
Notary Public

On this 13th day of February, 1986, before me, a Notary Public in and of the State and County aforesaid, personally appeared KARL SIMS, to me known and known to me to be the person of that name, who signed and sealed the foregoing instrument, and he acknowledged the same to be his free act and deed.

Barbara B. Wollam,
Notary Public